A Project Report on

## Design and Implementation of 4-bit Synchronous Up/Down Counter in ASIC Design Flow

Submitted in partial fulfillment of the requirements for the award of the Degree of

**HONORS**

In

**ELECTRONICS AND COMMUNICATION ENGINEERING**

By

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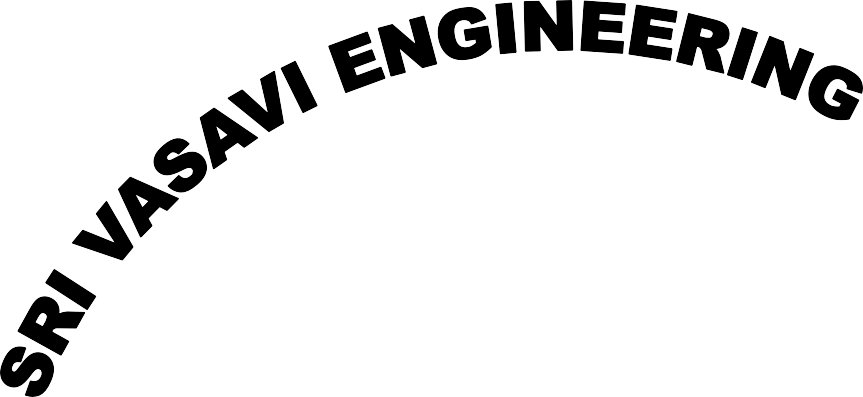
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**SRI VASAVI ENGINEERING COLLEGE (AUTONOMOUS)**

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# CERTIFICATE

This is to certify that the project report entitled “Design and Implementation of 4-bit Synchronous Up/Down Counter in ASIC Design Flow” being submitted by the students. **P. Lakshmi Charitha (21A85A0406)** in partial fulfillment for award of honor’s degree of **Bachelor of Technology** in **Electronics and Communication Engineering** for the academic year 2023-2024 from **Sri Vasavi Engineering College,** Tadepalligudem, affiliated to the **Jawaharlal Nehru Technological University, Kakinada (JNTUK),** Recognized by A.I.C.T.E, New Delhi, Accredited by NBA & NAAC with ‘A’ Grade is a record of bonafide work carried out by them under my guidance and supervision.

**PROJECT GUIDE HEAD OF THE DEPARTMENT**

(Mrs. Y.Sujatha) ( Dr. E. Kusuma Kumari)

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**PROJECT ASSOCIATE**

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# ABSTRACT

This project outlines the design and implementation of a 4-bit synchronous up/down counter using Cadence tools in the Application-Specific Integrated Circuit (ASIC) design flow. The counter exhibits versatility by supporting both incrementing and decrementing sequences, making it adaptable for various digital applications. The ASIC design flow, encompassing stages such as specification, simulation, synthesis, and verification, is systematically employed, highlighting the seamless integration of Cadence tools for efficient development. The paper addresses key design considerations, including clock synchronization, flip-flop selection, and optimized routing, to ensure reliable and high-performance operation in both counting directions. It emphasizes practical insights into bidirectional counter design and demonstrates the effectiveness of Cadence tools in creating a robust and versatile digital circuit. Simulation results confirm the counter's functionality, showcasing accurate timing behavior and adherence to design specifications in both up and down counting modes.

**Keywords**:- *Counter, Synchronization, reliable, Synthesis, RTL*

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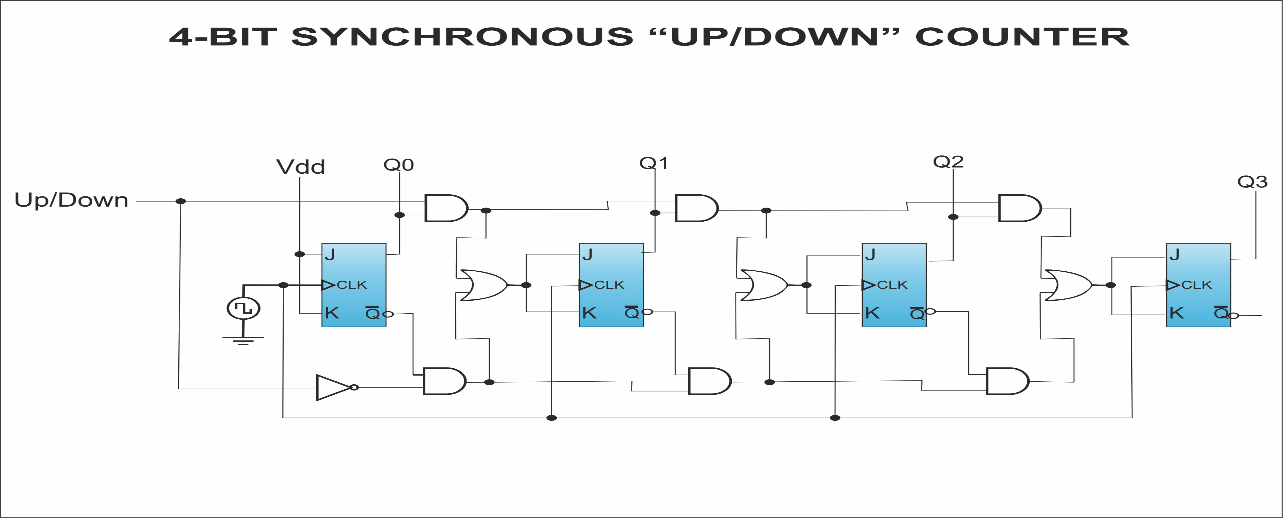
Table 1.1:- Truth table of Counter

**1. INTRODUCTION**

**Introduction to Synchronous Up/down Counter**

In the ever-evolving landscape of digital electronics, counters are fundamental components, integral to a wide array of applications such as pulse counting, frequency division, and state machine implementation. This project focuses on the design and implementation of a 4-bit synchronous up/down counter, employing the comprehensive ASIC (Application-Specific Integrated Circuit) design flow from Register Transfer Level (RTL) to Graphic Data System II (GDSII). The 4-bit synchronous up/down counter is a versatile digital device capable of counting in both ascending and descending order, controlled by external inputs. It progresses through a binary sequence from 0000 to 1111 in up mode and reverses the sequence from 1111 to 0000 in down mode. This bidirectional counting ability makes it essential for various digital applications, including digital clocks, programmable timers, and digital state machines.

**LOGIC DIAGRAM OF 4-BIT SYNCHRONOUS UP/DOWN COUNTER**



***Fig 1.1 Logic Diagram of 4-bit Synchronous UP/DOWN Counter***

A 4-bit synchronous up/down counter is a digital circuit that can count both upwards and downwards, depending on a control input signal. Each state change in the counter is synchronized with a clock signal, meaning all flip-flops in the counter change state simultaneously in response to the clock.

**Key Components of a 4-bit Synchronous Up/Down Counter:**

**1**. **Flip-Flops:** Typically, JK or D flip-flops are used, with four flip-flops representing the four bits.

**2**. **Control Signal (UP/DOWN**): Determines the counting direction. When this signal is high, the counter counts up; when low, it counts down.

**3. Clock Signal**: Synchronizes the state changes of the counter.

**4. Logic Gates**: Used to control the counting operation based on the control signal.

**Working Principle:**

Counting Up:

- When the UP/DOWN control signal is high, the counter counts up from 0000 to 1111.

- On each clock pulse, the counter increments its value by one.

Counting Down:

- When the UP/DOWN control signal is low, the counter counts down from 1111 to 0000.

- On each clock pulse, the counter decrements its value by one.

**TRUTH TABLE**

|  |  |  |  |
| --- | --- | --- | --- |
| **CLOCK** | **RESET** | **CONTROL INPUT(M)** | **OUTPUT (COUNT)** |
| X | X | X | 0 |
| 1 | 1 | X | 0 |
| 1 | 0 | 0 | COUNT-1 |
| 1 | 0 | 1 | COUNT+1 |

***Table 1.1:- Truth table of Counter***

**TIMING DIAGRAM OF SYNCHRONOUS UP/DOWN COUNTER**

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***Fig1.2:- Timing Diagram of Synchronous Up/Down Counter***

**2. SOFTWARE REQUIREMENTS**

## 2.1 Introduction to CADENCE Software:

Cadence Design Systems provides a suite of electronic design automation (EDA) tools, which are software tools used in the design and development of electronic systems, including integrated circuits (ICs) and printed circuit boards (PCBs). Cadence provides tools that support both RTL (Register-Transfer Level) design and schematic entry, offering a comprehensive solution for designers working at different abstraction levels in the electronic design process.

For ASIC (Application-Specific Integrated Circuit) design flows, Cadence offers a comprehensive set of tools that cover various stages of the ASIC design process. The ASIC design flow involves steps such as RTL (Register-Transfer Level) design, synthesis, place and route, static timing analysis, and physical verification. Cadence's tools are designed to support these stages, providing a seamless and integrated environment for ASIC designers.

ASIC (Application-Specific Integrated Circuit) design involves a systematic process to create customized integrated circuits tailored for specific applications. The ASIC design flow encompasses various stages, from conceptualization to physical implementation.

**1. Specification and Conceptualization:** The design process begins with understanding the application requirements and defining the specifications for the ASIC. Designers outline the desired functionality, performance metrics, and any specific constraints.

**2. RTL Design:** Register-Transfer Level (RTL) design involves creating a high-level abstraction of the digital circuit using hardware description languages (HDLs) such as Verilog or VHDL.

Tools: Genus Synthesis Solution can be employed to perform logic synthesis, transforming RTL descriptions into gate-level netlists optimized for area, power, and performance.

**3. Functional Verification:** The RTL design undergoes thorough functional verification to ensure it meets the specified requirements and behaves as intended.

Tools: Functional verification tools such as simulation tools (e.g., VCS) and formal verification tools (e.g., Conformal) are used to validate the design.

**4. Synthesis and Optimization:** The RTL design is synthesized into gate-level netlists. Optimization techniques are applied to achieve the desired performance, power, and area (PPA) metrics.

Tools: Genus Synthesis Solution plays a crucial role in this stage, optimizing the design for PPA.

**5. Place and Route:** Physical implementation involves placing the logic elements and routing the interconnections on the chip's layout. This stage ensures that the design meets timing requirements and minimizes area.

Tools: Innovus Implementation System is used for place and route, clock tree synthesis, and optimization.

**6. Timing Analysis:** Static timing analysis is performed to ensure that the design meets timing constraints and operates within specified clock frequencies.

Tools: Tempus Timing Signoff Solution is commonly used for static timing analysis.

**7. Power Analysis and Optimization:** Power analysis is performed to assess and optimize the power consumption of the ASIC design.

Tools: Voltus IC Power Integrity Solution is utilized for power analysis and optimization.

**8. Physical Verification:** Design rule checking (DRC) and layout vs. schematic (LVS) verification are conducted to ensure that the physical layout adheres to manufacturing rules and matches the intended circuit functionality.

Tools: Physical Verification System (PVS) is used for DRC and LVS verification.

**9. Full-Chip Simulation:** Full-chip simulations are performed to validate the entire ASIC design under realistic conditions.

Tools: Tools like VCS can be employed for full-chip simulation.

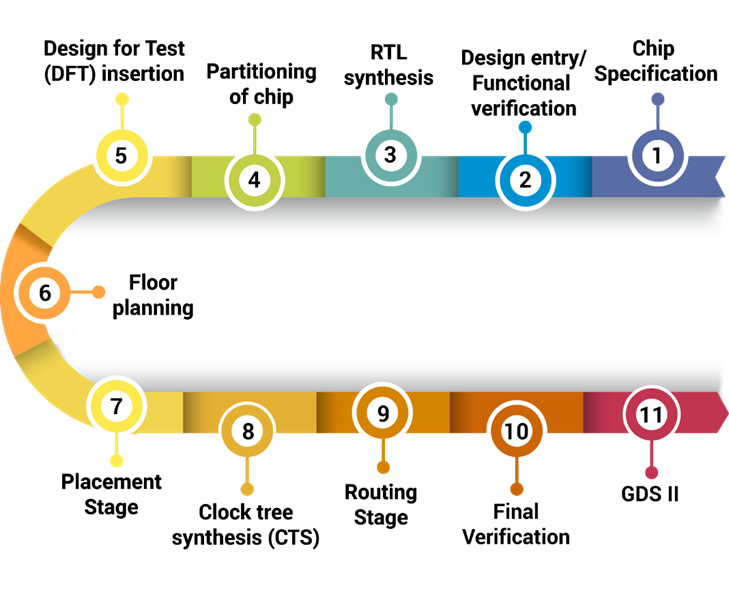
**10. Tapeout:** The finalized design is prepared for manufacturing, and the data is sent for fabrication (tapeout).Ensuring that the design adheres to foundry-specific guidelines and requirements is crucial for successful tapeout.

**11. Post-Silicon Validation:** After fabrication, the ASIC undergoes testing and validation to ensure it functions correctly in real-world conditions.

Tools: Depending on the application, specialized testing equipment and methodologies are used for post-silicon validation.

This comprehensive ASIC design flow involves a series of steps, tools, and methodologies to transform a concept into a physical ASIC. Each stage plays a crucial role in ensuring that the final ASIC meets the specified requirements and performs optimally in its intended application. The use of Cadence tools, such as Genus, Innovus, and others, provides a cohesive and integrated environment for designers to navigate through these stages efficiently.

## 2.2 ASIC DESIGN FLOW

******

***Fig 2.1:- ASIC Design Flow***

**System Specification:**

The first step of the VLSI Design Flow is system specifications. System specification is a high-level representation of the system. The factors to be considered in this process include performance, functionality, and interface.

**Architectural Design:** This is the step where the main work starts with the help of system specification. Design engineers design the architecture according to system specifications.

**Functional and Logic Design:**

In this step functionality of the design is identified. It specifies the hardware implementation of system functionality. The outcome of functional design is usually a timing diagram.

In the logic design step, register allocation, logic, and arithmetic operations of the design that represent the functional design are derived and tested this description is called RTL description. RTL stands for register transfer level. In this step, system specification is expressed in hardware description language (HDL) such as Verilog and VHDL.

RTL description is used for simulation to test the functionality with the help of EDA tools.

Functional verification is performed to ensure the RTL design is done according to the specifications. RTL code is converted to gate-level netlist using synthesis tools. Netlist is a description of the circuit in terms of gates and connections between them.

To verify whether the synthesis tool has correctly generated the gate-level netlist a verification should be done.

**Circuit Design:**

In this step circuit is designed based on the logic design. The Boolean expressions are converted into circuit representation by taking into consideration the power and speed requirements of the original design.

Circuit simulation is used to verify the correctness and timing of each component. Diagram consists of circuit elements such as gates and transistors.

**Physical Design:**

In this step, the netlist is converted into a physical geometric representation.

The layout is a representation of an IC in terms of planar geometric shapes that correspond to the patterns of metal oxide or semiconductor layers that make up the components of the Integrated circuit. The layout is designed by a tool such as Cadence Virtuoso.

Physical design is a very complex step therefore it is divided into sub-steps such as floor planning, placement, clock tree synthesis, routing, etc and timing analysis checks are formed in every step during physical design.

Floor planning is a process of placing the various blocks and the I/O pads across the chip area based on the design constraints.

Placement of physical elements within each block and integration of analog blocks or external IP cores is performed. When all the elements are placed, a global and detailed routing is running to connect all the elements.

The output of the layout is a GDSII file which is given to the foundry to fabricate the chip. The layout should be done according to foundry design rules.

**Physical Verification and Signoff:**

In this step, we perform physical verification checks such as Layout Vs schematic (LVS) and Design Rule check (DRC).

DRC verifies whether the given layout satisfies the design rules provided by the fabrication team. DRC checks are nothing but physical checks of spacing rules between metals, minimum width rules, via rules, etc.

LVS is a major check in the physical verification stage. Layout is compared with the schematic to verify whether their functional match or not. If it matches, then the LVS reports clean.

**Fabrication:**

After the physical verification step, the design is ready for fabrication. Tape out is the final result of the design process for integrated circuits before they are sent for manufacturing. The tape-out is specifically the point at which the graphic for the photo mask of the circuit is sent to the foundry.

The fabrication process consists of several steps involving wafer growth, epitaxial growth masking, etching, doping, deposition, and diffusion of various materials on the wafer. During each step, one mask is used.

**Packaging and Testing:**

Each of the wafers contains hundreds of chips. These chips are separated and packaged by a method called scribing and cleaving. The chips that fail in electrical tests are discarded.

Each chip is packaged and tested to ensure that it meets all the design specifications and functions properly.

**3. SIMULATION RESULTS**

## Verilog Code for the Counter

### `timescale 1ns/1ps module counter(count,clk,m,rst); input clk,rst,m; output reg[3:0] count; always@(posedge clk or negedge rst) begin if(!rst) count=0; else if(m) count=count+1; else count=count-1; end endmodule

### **Test bench Verilog Code**

timescale 1ns/1ps  
module counter\_tb();  
reg clk,m,rst;  
wire [3:0]count;  
counter x1(count,m,clk,rst);  
always  
begin  
#5 clk=~clk;  
end  
initial  
begin  
clk=0;  
rst=0;  
#5 rst=1;  
end  
initial  
begin  
m=1;  
#160 m=0;  
$display("time=%t rst=%b clk=%b count=%b", $time,rst,clk,count);  
$finish;  
end  
endmodule

### **TCL script for Synthesis:**

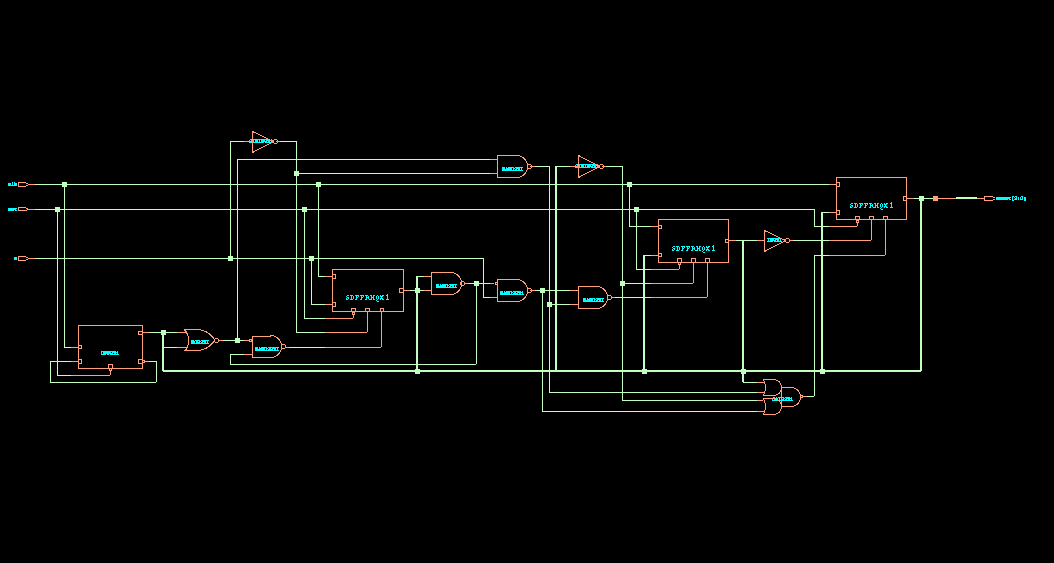
# liberty file path  
read\_libs /home/install/FOUNDRY/digital/90nm/dig/lib/slow.lib  
# top logic file name  
read\_hdl counter.v  
elaborate  
# sdc file name  
read\_sdc counter\_input.sdc  
# setting effort levels for 3 stages  
set\_db syn\_generic\_effort medium  
set\_db syn\_map\_effort medium  
set\_db syn\_opt\_effort medium  
# synthesis of generic gates  
syn\_generic  
# synthesising for mapping  
syn\_map  
# for optimization  
syn\_opt  
# for sequential circuits  
report\_timing > counter\_timing.repo  
# for combinational circuits

report\_timing -unconstrained > counter\_timing.repo  
# generating power report  
report\_power > counter\_power.repo  
# generating area report  
report\_area > counter\_area.repo  
# generating netlist from synthesis  
write\_hdl > counter\_netlist.v  
# generating sdc file from synthesis  
write\_sdc > counter\_output.sdc  
# to see the schematic  
gui\_show

### **Synopsys Design Constraints file for Synthesis**

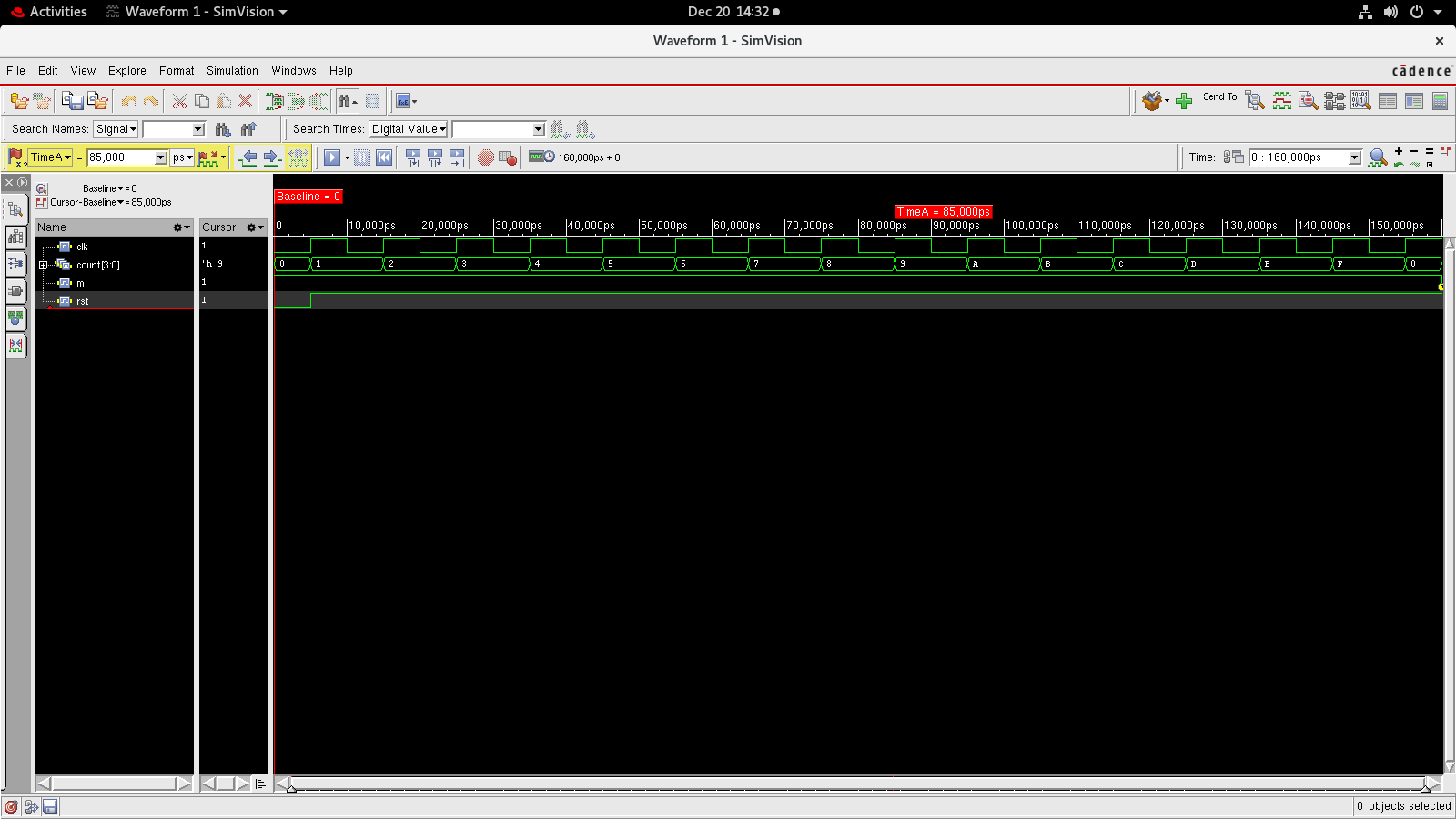
create\_clock -name clk -period 2 -waveform {0 1} [get\_ports "clk"]  
set\_clock\_transition -rise 0.1 [get\_clocks "clk"]  
set\_clock\_transition -fall 0.1 [get\_clocks "clk"]  
set\_clock\_uncertainity 0.01 [get\_ports "clk"]  
set\_input\_transition 0.12 [all\_inputs]  
set\_input\_delay -max 0.8 [get\_ports "clk"] -clock [get\_clocks "clk"]  
set\_input\_delay -max 0.8 [get\_ports "m"] -clock [get\_clocks "clk"]  
set\_input\_delay -max 0.8 [get\_ports "rst"] -clock [get\_clocks "clk"]  
set\_output\_delay -max 0.8 [get\_ports "count"] -clock [get\_clocks "clk"]

**Schematic View of Counter**

**

***Fig 3.1 Schematic view of Counter***

**Output Waveforms**



***Fig 3.2:- Output Waveforms of Counter***

## 3.1 Design Metric Analysis:

### **Area**

============================================================

Generated by: Genus(TM) Synthesis Solution 21.14-s082\_1

Generated on: Dec 18 2023 02:48:56 pm

Module: counter

Operating conditions: slow (balanced\_tree)

Wireload mode: enclosed

Area mode: timing library

============================================================

Instance Module Cell Count Cell Area Net Area Total Area Wireload

--------------------------------------------------------------------------

counter 13 132.457 0.000 132.457 <none> (D)

(D) = wireload is default in technology library

**Power**

Instance: /counter

Power Unit: W

PDB Frames: /stim#0/frame#0

----------------------------------------------------------------------------------------------

Category Leakage Internal Switching Total Row%

--------------------------------------------------------------------------------------------

memory 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%

register 5.31456e-07 4.53673e-05 1.14874e-06 4.70475e-05 84.64%

latch 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%

logic 2.28281e-07 3.22999e-06 2.32515e-06 5.78342e-06 10.40%

bbox 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%

clock 0.00000e+00 0.00000e+00 2.75400e-06 2.75400e-06 4.95%

pad 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%

pm 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%

----------------------------------------------------------------------------------------------

Subtotal 7.59737e-07 4.85973e-05 6.22789e-06 5.55849e-05 99.99%

Percentage 1.37% 87.43% 11.20% 100.00% 100.00%

-----------------------------------------------------------------------------------------------

**Timing**

============================================================

Generated by: Genus(TM) Synthesis Solution 21.14-s082\_1

Generated on: Dec 18 2023 02:48:56 pm

Module: counter

Operating conditions: slow (balanced\_tree)

Wireload mode: enclosed

Area mode: timing library

============================================================

Path 1: UNCONSTRAINED Setup Check with Pin count\_reg[3]/CK->SE

Startpoint: (F) n

Endpoint: (F) count\_reg[3]/SE

Clock: (R) -

Capture Launch

Drv Adjust:+ 0 0

Setup:- 290

Data Path:- 449

#----------------------------------------------------------------------------------------

# Timing Point Flags Arc Edge Cell Fanout Load Trans Delay Arrival

# (fF) (ps) (ps) (ps)

#----------------------------------------------------------------------------------------

n - - F (arrival) 4 10.0 120 0 0

g243\_\_5526/Y - A->Y F OR3XL 3 6.4 118 252 252

g239\_\_5107/Y - B->Y F MX2X1 1 4.9 73 197 449

count\_reg[3]/SE - - F SDFFRHQX1 1 - - 0 449

#----------------------------------------------------------------------------------------

**GDS FILE**

****

***Fig 3.3:- GDS File of Counter***

**4. ADVANTAGES AND APPLICATIONS**

**4.1 Advantages of Synchronous Up/Down Counters**

**1. Precision and Reliability:**

**Clock Synchronization:** All flip-flops are driven by a common clock signal, reducing timing errors and ensuring synchronized counting.

**Predictable Timing**: Synchronous operation ensures that all state changes occur simultaneously with the clock edge, leading to predictable and reliable timing.

**2. Scalability:**

**Ease of Expansion:** Adding more bits to the counter is straightforward as each additional flip-flop integrates seamlessly with the existing design.

**Design Modularity:** The modular nature of synchronous counters makes them easier to design, debug, and expand.

**3**. **Simplified Design:**

**Reduced Complexity:** The use of a common clock simplifies the design and reduces the complexity of the control logic compared to asynchronous counters.

**Ease of Implementation**: Synchronous counters can be easily implemented using standard flip-flops and logic gates.

**4. Performance:**

**High Speed:** The synchronous operation allows for higher operating speeds since all changes are aligned with the clock.

**Minimal Glitches:** Synchronous counters are less prone to glitches and race conditions, ensuring more stable and accurate counting.

**4.2 Applications of Synchronous Up/Down Counters**

**1. Digital Systems:**

**Microprocessors and Microcontrollers**: Used for program counters, timers, and event counters.

**Memory Addressing**: Employed in RAM and ROM modules for address sequencing.

**2. Timing and Control:**

**Clock Dividers:** Used to generate specific time intervals by dividing the clock frequency.

**Frequency Counters**: Measure the frequency of input signals in communication systems and oscilloscopes.

**3. Data Processing:**

**Arithmetic Operations:** Serve as building blocks for arithmetic units, performing operations like addition and subtraction.

**State Machines:** Implement finite state machines for control applications in embedded systems.

**4.** **Industrial and Consumer Electronics:**

**Automation Systems:** Used in programmable logic controllers (PLCs) for counting parts or events.

**Digital Watches and Clocks**: Implement timekeeping functions, counting seconds, minutes, and hours.

**5. Communication Systems:**

**Channel Selection:** Used in frequency synthesizers for tuning radio frequencies.

**Error Detection:** Employed in cyclic redundancy check (CRC) circuits for error detection and correction.

**6.** **Display Systems:**

**LED and LCD Displays:** Drive display modules for counting and displaying numerical information.

**5.CONCLUSION**

**5.1 Conclusion**

The project aimed to design and implement a 4-bit up/down counter using the ASIC design flow from RTL to GDSII with Cadence tools. Functional simulation with Xcelium verified the RTL code's correctness, ensuring accurate counting functionality. Synthesis with Genus translated the RTL to a gate-level netlist, optimizing for area, power, and timing, resulting in metrics of 132.457 units for area, 55.5849 microwatts for power, and 197 picoseconds for delay, with a datapath length of 449. Physical design using Innovus included floorplanning, placement, CTS, routing, and optimization, leading to a manufacturable GDSII file. The design achieved a compact area, low power consumption, and fast performance, demonstrating efficient use of silicon and suitability for low-power applications. The project successfully balanced area, power, and performance, showcasing effective use of Cadence tools and providing a solid foundation for integrating the counter into larger systems. Overall, the project demonstrates the effectiveness of using Cadence tools for ASIC design, from initial RTL coding to the final GDSII file generation. The results indicate that the design is well-optimized, balancing area, power, and performance metrics, making it suitable for integration into larger systems where a reliable and efficient 4-bit up/down counter is required. This project serves as a solid foundation for more complex digital designs and highlights the importance of each step in the ASIC design flow.